

US Microelectronics Packaging Ecosystem: Challenges and Opportunities

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Abstract—The semiconductor industry is experiencing a significant shift from traditional methods of shrinking devices and reducing costs. Chip designers actively seek new technological solutions to enhance cost-effectiveness while incorporating more features into the silicon footprint. One promising approach is Heterogeneous Integration (HI), which involves advanced packaging techniques to integrate independently designed and manufactured components using the most suitable process technology. However, adopting HI introduces design and security challenges. To enable HI, research and development of advanced packaging is crucial. The existing research raises the possible security threats in the advanced packaging supply chain, as most of the Outsourced Semiconductor Assembly and Test (OSAT) facilities/vendors are offshore. To deal with the increasing demand for semiconductors and to ensure a secure semiconductor supply chain, there are sizable efforts from the United States (US) government to bring semiconductor fabrication facilities onshore. However, the US-based advanced packaging capabilities must also be ramped up to fully realize the vision of establishing a secure, efficient, resilient semiconductor supply chain. Our effort was motivated to identify the possible bottlenecks and weak links in the advanced packaging supply chain based in the US.

Index Terms—Advanced Packaging, Semiconductor Supply Chain, Advanced Packaging Supply Chain, Hardware Security and Assurance, Secure Heterogeneous Integration.

I. INTRODUCTION

The pervasive presence of electronic devices is profoundly transforming our way of life and work, becoming deeply embedded in our daily routines. In today's digital-driven economy, the widespread use of high-speed devices and seamless connectivity generates an immense volume of data. Various critical systems, including autonomous cars, data centers, and Artificial Intelligence (AI) systems, rely on capturing, storing, and analyzing this big data to enable data-driven transactions. Integrated Circuits (ICs) play a pivotal role in supporting the evolution of data processing, high-performance computing, and wireless communication. Today's cutting-edge ICs provide high-bandwidth memory, multiple processing cores, and high-speed input/output (I/O) ports. The presence of these cutting-edge ICs can be primarily credited to Moore's Law, which has driven the semiconductor sector to consistently produce ICs that are faster, smaller, and more cost-effective. However, this long-standing law faces limitations due to rising fabrication

costs, power dissipation challenges, and yield issues associated with advanced technology nodes.

In response to the hurdles encountered in the traditional scaling of CMOS technology, the International Technology Roadmap for Semiconductors (ITRS) 2015 introduced a forward-looking strategy to sustain the historical advancement of CMOS technology [1]. This vision centers around adopting HI as a viable solution. HI involves integrating individually designed and fabricated components on a substrate layer known as an interposer, allowing them to function like a System on Chip (SoC) collectively.

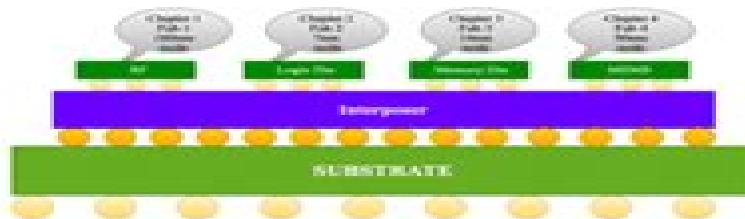


Fig. 1: System-in-Package (SiP) for HI

HI amalgamates separately manufactured components with varying technology nodes and functionalities, resulting in a more advanced assembly known as a Multi-Chip Module (MCM) or System in Package (SiP) (Fig. 1). SiPs offer expanded functionality and improved operational characteristics that are difficult to accomplish with a single-die SoC approach. Diverse components, such as chiplets, active/passive parts, and MEMS devices, can be integrated as a unified package into the SiP. Chiplets, for example, are individually fabricated silicon dies [2] designed explicitly for targeted functions like memory, analog-mixed signal processing, radio frequency (RF), or processors. The SiP can be integrated through adjacent placement (2.5D) or vertical stacking (3D) of chiplets on the interposer.

While HI offers numerous advantages, further research and development are needed to enhance its effectiveness. To realize the vision of HI and continue Moore's Law, packaging technology needs to be improved to standardize intercon-

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Modeling and Simulation for Microelectronic Packaging Assembly Shen Liu, Yong Liu, 2011-05-17 Although there is increasing need for modeling and simulation in the IC package design phase most assembly processes and various reliability tests are still based on the time consuming test and try out method to obtain the best solution. Modeling and simulation can easily ensure virtual Design of Experiments (DoE) to achieve the optimal solution. This has greatly reduced the cost and production time especially for new product development. Using modeling and simulation will become increasingly necessary for future advances in 3D package development. In this book Liu and Liu allow people in the area to learn the basic and advanced modeling and simulation skills to help solve problems they encounter. Models and simulations numerous processes in manufacturing reliability and testing for the first time. Provides the skills necessary for virtual prototyping and virtual reliability qualification and testing. Demonstrates concurrent engineering and co design approaches for advanced engineering design of microelectronic products. Covers packaging and assembly for typical ICs, optoelectronics, MEMS, 2D, 3D, SiP and nano interconnects. Appendix and color images available for download from the book's companion website. Liu and Liu have optimized the book for practicing engineers, researchers, and post graduates in microelectronic packaging and interconnection design assembly, manufacturing, electronic reliability, quality, and semiconductor materials. Product managers, application engineers, sales and marketing staff who need to explain to customers how the assembly manufacturing reliability and testing will impact their products will also find this book a critical resource. Appendix and color version of selected figures can be found at www.wiley.com/go/liu/packaging

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